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EXAMINER

STOYNOV, STEFAN

ART UNIT PAPER NUMBER

2116

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/027,652

Applicant(s)

COOPER, BARNES

Examiner

Stefan Stoynov

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-10, 17-20 and 27-30 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 11-13, 16, 21-23 and 26 is/are rejected.
- 7) ☒ Claim(s) 5, 14, 15, 24 and 25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

The rejections are respectfully maintained and reproduced infra for applicant's convenience.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 4, 13, and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3, 13, and 23 depend on claims 1, 11, and 21 where alternative language is used to describe updating the performance state structure using either a processor performance table or a default table.

Whereas, claims 3, 13, and 23 imply the presence for both a processor performance table and default table. Accordingly, it is unclear what elements are required by the claims.

If the applicant desires the presence for both the performance table and the default table, claims 1, 11, and 21 need to be modified to account for that.

Claim 4 is similarly indefinite being dependent on claim 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 6, 11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osborn et al., U.S. Patent No. 6,721,892 in view of Barrus, U.S. Patent No. 5,958,058.

Re claims 1 and 11, Osborn discloses a method and computer program product comprising:

reading a performance information associated with a processor (column 5, lines 5-7, lines 21-24, lines 54-57, FIG. 1);

Osborn does not specifically state reading the performance information. However, Osborn discloses the performance information associated with the functional unit (e.g. processor) being received by the performance control adjustment circuit (column 5, lines 54-57) and based on this information, the control circuit initiates the required performance adjustments. Thus, the control circuit reads the performance information, and thus Osborn discloses reading a performance information associated with a processor.

attempting to locate a processor performance table that corresponds to the performance information (column 9, lines 50-53, lines 61-66, FIG. 6), the performance

table including a plurality of performance parameters to control the performance of the processor (column 9, lines 50-57, lines 61-67, column 7, lines 1-22, FIG. 6);

Osborn fails to disclose updating a performance state (PS) structure using one of the processor performance table and a default table.

Barrus teaches a power management utility program (column 2, line 26) using an application requirement data structure which contains the hardware performance parameters that enable each of the applications on the computer to run at desired level (column 4 lines 62-67, column 5, lines 1-3). Barrus further teaches updating the performance requirements in the data structure (column 5, lines 21-26). In Barrus, the power management utility program incorporating the application requirement data structure assists the user in selecting hardware performance settings to optimize battery life and also to monitor whether the settings are sufficient to run software applications with desired effectiveness (column 3, line 24-28), thus maximizing both battery life and software performance (column 2, lines 25-29).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the application requirement data structure and the process of updating it, as suggested by Barrus with the method and computer program product disclosed by Osborn in order to implement updating a performance state (PS) structure using one of the processor performance table and a default table, thus maximizing both battery life and software performance.

Re claims 6 and 16, Osborn further teaches the method and computer program product wherein reading the performance information comprises:

reading a bus ratio parameter and a voltage identifier (FIG. 6), the bus ratio parameter corresponding to an operating frequency, the voltage identifier corresponding to an operating power of the processor (column 5, lines 43-67).

Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osborn et al., U.S. Patent No. 6,721,892 in view of Barrus, U.S. Patent No. 5,958,058, and further in view of Berc et al., U.S. Patent No. 5,796,939.

Re claims 2 and 12, Osborn and Barrus disclose the method and computer program product as per claims 1 and 11. In addition Barrus further teaches reading one of a maximum performance parameter and a minimum performance parameter (column 8, lines 48-52, column 9, lines 8-11).

Osborn and Barrus fail to disclose reading the performance parameter from a register in the processor.

Berc teaches collecting performance data in a computer system (column 1, lines 5-7). Berc further teaches a set of counters or registers associated with the processor, co-resident on the same semiconductor die (column 4, lines 1-6, FIG. 2, 201). Each of the registers stores a count for performance events (column 4, lines 7-8) and is sampled in response to interrupts generated by an interrupt handler (column 2, lines 5-7). In Berc, the performance monitoring utilizing the performance registers allows for very high sampling rate and minimizes the overhead to a minimum, thus achieving accurate evaluation for the system's performance (column 1, lines 52-57).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the performance registers, as suggested by Berc for the

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method and computer program product disclosed by Osborn and Barrus in order to implement reading the performance parameter from a register in the processor, thus achieving accurate evaluation for the system's performance.

Claims 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osborn et al., U.S. Patent No. 6,721,892 in view of Barrus, U.S. Patent No. 5,958,058, and further in view of Hobson, U.S. Patent No. 6,112,164.

Re claim 21, Osborn and Barrus disclose all claim limitations as per claim 1. In addition, Osborn further discloses a processor (FIG. 4) and a memory coupled to the processor (FIG. 4).

Osborn and Barrus fail to disclose a memory storing a system management interrupt (SMI) handler, the SMI handler executing in response to an SMI.

Hobson teaches storing the SMI handler program code (column 3, line 3) in different types of nonvolatile memory (column 4, lines 50-54). Hobson further teaches a timer generating a SMI, which invokes a SMI handler that determines if one of the software thermal thresholds has been crossed (column 2, line 67, column 3, lines 1-4). If one of the thresholds has been crossed, the software thermal bracket is adjusted and the ACPI operating system is informed of the thermal event (column 3, lines 4-10). The ACPI operating system then processes the event according with a predetermined thermal policy (column 3, lines 4-12). In Hobson, the method of using the SMI handler allows for legacy computer systems having a one-shot thermal device to implement ACPI thermal management procedures.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use a SMI handler stored in nonvolatile memory, invoking the SMI handler in response to a SMI, and informing the ACPI operating system of a thermal event, as suggested by Hobson for the system disclosed by Osborn and Barrus in order to implement a memory storing a system management interrupt (SMI) handler, the SMI handler executing in response to a SMI, thus allowing for legacy computer systems having a one-shot thermal device to implement ACPI thermal management procedures.

Re claim 26, Osborn further teaches the system wherein the SMI handler causing the processor to read the performance information causes the processor to:

read a bus ratio parameter and a voltage identifier (FIG. 6), the bus ratio parameter corresponding to an operating frequency, the voltage identifier corresponding to an operating power of the processor (column 5, lines 43-67).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Osborn et al., U.S. Patent No. 6,721,892 in view of Barrus, U.S. Patent No. 5,958,058, further in view of Hobson, U.S. Patent No. 6,112,164, and further in view of Berc et al., U.S. Patent No. 5,796,939.

Re claim 22, Osborn, Barrus, and Hobson disclose the system as per claim 21. In addition Barrus further teaches reading one of a maximum performance parameter and a minimum performance parameter (column 8, lines 48-52, column 9, lines 8-11).

Osborn, Barrus, and Hobson fail to disclose reading the performance parameter from a register in the processor.

Berc teaches collecting performance data in a computer system (column 1, lines 5-7). Berc further teaches a set of counters or registers associated with the processor, co-resident on the same semiconductor die (column 4, lines 1-6, FIG. 2, 201). Each of the registers stores a count for performance events (column 4, lines 7-8) and is sampled in response to interrupts generated by an interrupt handler (column 2, lines 5-7). In Berc, the performance monitoring utilizing the performance registers allows for very high sampling rate and minimizes the overhead to a minimum, thus achieving accurate evaluation for the system's performance (column 1, lines 52-57).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the performance registers, as suggested by Berc for the method and computer program product disclosed by Osborn, Barrus, and Hobson in order to implement reading the performance parameter from a register in the processor, thus achieving accurate evaluation for the system's performance.

Allowable Subject Matter

Claims 17-20 are allowed.

Claims 3, 4, 13, and 23 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 5, 14, 15, 24, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The allowable subject matter for claims 5, 24, and 25 was addressed in the previous office action.

Re claim 14, the prior art fails to disclose or suggest, alone or in combination, the computer program product as per claim 11, comprising "computer readable program code to parse a sores language code containing the PS structure; and computer readable program code to replace entries in the PS structure by the local table".

Re claim 15, the prior art fails to disclose or suggest, alone or in combination, the computer program product as per claim 11, comprising "computer readable program code to update a checksum for a description table according to an advanced configuration and power management (ACPI) protocol".

Re claim 17, the prior art fails to disclose or suggest, alone or in combination, a computer program product comprising "computer readable program code to boot a platform having a processor after a performance state (PS) structure is updated with one of a processor performance table and a default table, the processor performance table being located based on processor information and including a plurality of performance parameters to control performance of the processor".

Response to Arguments

The examiner agrees with applicant's argument that claims 11-20 cover statutory subject matter. The rejection under 35 U.S.C. § 101 has been withdrawn.

The examiner respectfully disagrees with applicant's argument with regards to claims 3, 4, 13, and 23 for the reasons stated above. Claims 3, 4, 13, and 23 stand rejected under 35 U.S.C. § 112, second paragraph.

The examiner agrees that Osborn does not teach or suggest attempting to locate a processor performance table corresponding to the communication rate and that Osborn discloses only one table. However, claims 1, 11, and 21 do not recite attempting to locate a processor performance table corresponding to the communication rate. In addition, claims 1, 11, and 21 do not recite a plurality or multiple performance tables, as argued by applicant. Thus, Osborn meets the claim language.

The examiner respectfully disagrees with applicant's argument with respect to combining Barrus with Osborn. The examiner agrees, that in one of the embodiments, the table is loaded into the data structure upon initialization. However, Barrus teaches alternative means for updating the data structure based on processor's performance information (column 5, lines 14-26). Thus, the combination of Barrus with Osborn meets the claim language for claims 1, 11, and 21.

Dependant claims 2, 6, 12, 16, 22, and 26 stand rejected on the grounds presented in the previous office action.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoykov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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